REMARKS

In the Official Action mailed 23 August 2005, the Examiner objected to the Drawings. The Examiner reviewed claims 1-29. The Examiner has objected to claims 3, 5-7, 18 and 20-22 for informalities; has objected to claims 2 and 16 for informalities; has objected to claims 15 and 29 for informalities; has rejected claims 1-9, 14, 17, 18-23, 28 and 29 under 35 U.S.C. §103(a); has rejected claims 10, 16 and 24 under 35 U.S.C. §103(a); has rejected 11-13 and 25-27 under 35 U.S.C. §103(a); and has rejected claims 15 under 35 U.S.C. §103(a).

Applicant has amended claims 1, 15, 17 and 29. Claims 1-29 remain pending.

The Examiner's objections and rejections are respectfully traversed below.

Objection to the Drawings

The Examiner has objected to the drawings as failing to comply with 37 C.F.R. §1.84(p)(5) because they include the reference characters not mentioned in the description (Figure 1 - WL1, WL2, WLn), and do not include the reference sign "89" mentioned in the description on page 8.

Applicant has amended paragraph [0027] to refer to the word lines WL1, WL2, ..., WLn shown in Fig. 1.

Also, Applicant has amended Paragraph [0033] of the specification (page 8) to correct the reference from "89" to -- 84 --.

Accordingly, reconsideration of the objections to the drawings as amended is respectfully requested.

Objection to Claims 3, 5-7, 18 and 20-22 for Informalities

The Examiner has objected to claims 3, 5-7, 18 and 20-22 for informalities. The Examiner indicates that the word "about" in these claims is indefinite. Applicant respectfully requests reconsideration.

Claims 3, 5, 18 and 20 refer to thicknesses of dielectrics of between about 30 and about 70 nanometers. It is clear from the specification that these thicknesses have been determined based on the response of the dielectric layer to bias potentials during programming. Because implementation of test structures with small variations in thickness needed to discover more precise limits on the ranges is impractical; because measurement of variations is difficult at these dimensions, and because the precise cutoffs of the range might only be determined within the

ability to detect variations in performance during programming over small variations in thicknesses, given the purpose of defining the ranges that is clear from the specification, it is in fact more accurate to refer to these ranges as approximate values, using the term "about," than as absolute limitations. It is submitted that persons of skill in this art will readily understand the claim as a whole, in view of the specification herein. See, MPEP 2173.05(b) Relative Terminology, A. "About".

Claims 6, 7, 21 and 22 refer to bias voltages of about 15 Volts over a small distance, in order to indicate a magnitude of the electric field across the dielectric layers. Again, the term "about" is in fact the more accurate way to claim the phenomenon that would a more absolute voltage level. Persons of skill in this art understand that slight variations in the voltage level may have no effect on the programming performance, and such performance depends on a number of variables related to bias voltages and cell structure, and a more specific value would be very difficult to develop. Id.

Accordingly, reconsideration of the objection to claims 3, 5-7, 18 and 20-22 is respectfully requested.

Objection to Claims 2 and 16 for Informalities

The Examiner has objected to claims 2 and 16 for informalities. The Examiner indicates that the phrase "sufficient to prevent direct tunneling" in these claims is indefinite. The claim reads on a thickness that is effective for a specific function recited in the claim and explained in the specification. Therefore, it is submitted that persons of skill in the art will understand the claim, and can determine what thicknesses are sufficient for the recited purpose. Accordingly, the claims are believed clear for the reasons explained in MPEP 2173.05(c) Numerical Ranges and Amounts Limitations, III. "Effective Amount".

Accordingly, reconsideration of the objection to claims 2 and 16 is respectfully requested.

Objection to Claims 15 and 29 for Informalities

The Examiner has objected to claims 15 and 29 for informalities. The Examiner indicates that the scope of the phrases "one or more," "other oxide material" and "etc." in these claims is indefinite. Applicant has amended such claims to address the objection.

Accordingly, reconsideration of the objection to claims 15 and 29 as amended is respectfully requested.

Rejection of Claims 1-9, 14, 17, 18-23, 28 and 29 under 35 U.S.C. §103(a)

The Examiner has rejected claims 1-9, 14, 17, 18-23, 28 and 29 under 35 U.S.C. §103(a) as being unpatentable over US Patent to Sakui et al. (6,307,807) in view of non-patent literature submitted by the applicant (Lee et al., "A Novel Structure of $SiNO_2$/SiN/High k Dielectrics, Al_2O_3 for SONOS Type Flash Memory," Extended Abstracts of the 2002 International Conference on Solid State Device and Materials, Nagoya (2002), 162-163). Reconsideration is respectfully requested.

Applicant has amended independent claims 1 and 17 to recite that the circuitry for programming and the logic for programming respectively operate "while limiting program and erase cycling." As described throughout the specification of the present application, operating without an erase cycle or with only a few erase cycles, prevents program and erase cycling damage to the tunneling dielectric that otherwise causes data retention problems in SONOS and SANOS cells. No references in the record suggest use of a SONOS or SANOS type cell with limited erase operations to prevent such damage by, as described in the application, operating the device as a read-only memory with no erase function or erase functions that support only a limited number of erase cycles. See, specification paragraph [0032]. Therefore, the combination relied upon by the Examiner does not result in the claimed invention.

Furthermore, the Examiner has made a mistake in asserting a motivation to combine the references. In particular, the Examiner asserts that one would apply the SONOS or SANOS cell structure in the architecture of Sakui et al. in order to solve charge loss problems with direct tunneling in SONOS cells. Sakui et al. describes NAND style flash memory using floating gate memory cells. No direct tunneling issues appear in floating gate style memory devices and it would not make sense to replace a cell with good data retention with a SONOS or SANOS cell with poor retention properties, in order to "solve charge loss problems." To make the Examiner's combination would have the opposite effect on the structure of Sakui et al., and cause worse performance.

Indeed, Sakui et al. specifically teaches away from use of a SONOS type cell at column 23, lines 27-52, where an article by Lancaster et al. is cited and distinguished. See, accompanying information disclosure with a copy of Lancaster et al. Sakui et al argues that the Sakui et al. invention provides "a remarkable effect different from those of ... the memory cell in [Lancaster et al]..." . Thus, persons of skill in the art would not be led to substitute the cells from Lee et al. with inferior charge retention characteristics, for the floating gate cells in Sakui et al.

Therefore, the Examiner has based the support for motivation to combine Sakui et al with Lee et al. on a mistake in fact. Furthermore, even if the references were combined, the resulting structure would not have circuitry or logic that limits program and erase cycling as set out in claims 1 and 17, as amended.

Claims 2-9 and 14 depend from claim 1 as amended, and are patentable for the same reasons, and because of the unique combinations recited. Likewise, claims 18-23 and 28-29 depend from claim 17 as amended, and are patentable for the same reasons, and because of the unique combinations recited.

We note further that with respect to claim 8, the Examiner is mistaken in characterizing column 1, lines 12-16 of Sakui et al. as suggesting a read-only memory. With respect to claims 9 and 23, the teaching of a negative threshold voltage by Sakui et al. for the floating gate cell would seem irrelevant if, as the Examiner has suggested, the cell of Sakui et al were replaced by a cell as taught in Lee et al.

Accordingly, reconsideration of the rejection of claims 1-9, 14, 17, 18-23, 28 and 29 as amended is respectfully requested.

Rejection of Claims 10, 16 and 24 under 35 U.S.C. §103(a)

The Examiner has rejected claims 10, 16 and 24 under 35 U.S.C. §103(a) as being unpatentable over Sakui et al. in view of Lee et al., and further in view of US Patent to Eitan (5,768,192).

Claims 10, 16 and 24 limit the invention to one-time programming.

Claim 10 depends from claim 1, and is patentable for the same reasons, and because of the unique combination recited. Claim 24 depends from claim 17, and is patentable for the same reasons, and because of the unique combination recited. Claim 16 is an independent claim which recites a memory cell structure.

As argued above, Sakui et al. and Lee et al. combined do not suggest configuring a memory for one-time programming, or otherwise limiting erase cycles, to avoid damage to the tunnel dielectric in the memory cell as described herein. The Examiner relies on Eitan to suggest this configuration. However, the combination does not make sense. If one replaced the cell of Sakui et al. with the cell in Lee et al., one would not then modify the circuit again with the structure of Eitan. One might apply Eitan to Lee et al. or apply Eitan to Sakui et al., but it is not clear how one would make a combination of all three.

Furthermore, Eitan teaches using an NROM style device as a programmable read only memory where the programming is accomplished using hot electron channel injection (See, Eitan, column 2, lines 53-58). This combination therefore leads away from the present invention as recited in claim 10, 16 and 24, and does not result in the claimed invention, in which programming is accomplished by the bias arrangement recited in the claims that causes E-field assisted tunneling.

Accordingly, reconsideration of the rejection of claims 10, 16 and 24 is respectfully requested.

Rejection of Claims 11-13 and 25-27 under 35 U.S.C. §103(a)

The Examiner has rejected claims 11-13 and 25-27 under 35 U.S.C. §103(a) as being unpatentable over Sakui et al. in view of Lee et al., and further in view of US Patent to Johnson et al. (5,343,437). Claims 11-13 depend from claim 1, and are patentable for the same reasons, and because of the unique combinations recited. Claims 25-27 depend from claim 17, and are patentable for the same reasons, and because of the unique combinations recited.

Accordingly, reconsideration of the rejection of claims 11-13 and 25-27 is respectfully requested.

Rejection of Claim 15 under 35 U.S.C. §103(a)

The Examiner has rejected claim 15 under 35 U.S.C. §103(a) as being unpatentable over Sakui et al. in view of Lee et al., and further in view of the non-patent literature (Liao et al., "Process Techniques and Electrical Characterization for High-k (HfO_xN_y) Gate Dielectric in MOS Devices," Proceedings, 7th International Conference on Solid-State and Integrated Circuits Technology, Volume 1, Oct. 2004, 372-377). Claim 15 depends from claim 1, and is patentable for the same reasons, and because of the unique combination recited.

Accordingly, reconsideration of the rejection of claim 15 as amended is respectfully requested.

CONCLUSION

It is respectfully submitted that this application is now in condition for allowance, and such action is requested.

Application No. 10/771,023

MXIC 1564-1
(P920205US)

The Commissioner is hereby authorized to charge any fee determined to be due in connection with this communication, or credit any overpayment, to our Deposit Account No. 50-0869 (MXIC 1564-1).

Respectfully submitted,

Dated: 23 November 2005

Mark A. Haynes, Reg. No. 30,846

HAYNES BEFFEL & WOLFELD LLP
P.O. Box 366
Half Moon Bay, CA 94019
(650) 712-0340 phone
(650) 712-0263 fax